

ABSTRACT OF THE DISCLOSURE

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Systems and methods allow driving a solid-state image pickup apparatus at high-speed operation by reducing a number of different samples in the horizontal and vertical directions. In an exemplary embodiment, three or more odd-numbered pixels are incorporated into a single block and signal charges from same color outputs are added within transfer registers such that an average center of the pixels coincides with a pixel at a center of the block. Three transfer electrodes are preferably provided for a column of a vertical transfer register in a part of the vertical transfer register on a side of the horizontal transfer register. The three transfer electrodes may be formed from one layer of three different gate electrode layers. The vertical registers may be arranged in a three column cycle. Preferably, an imaging device employing this structure has a switching mode of operation between a mode in which mixed charges that result from adding signal charges of predetermined pixels from one block are output and a normal mode for outputting all pixel information.